PCIM-DAS1602/16

Specifications

Document Revision 1.1, February, 2010

Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Power consumption

+5V quiescent	820mA typical, 1.4A max

Analog input

A/D converter type	LTC1605CSW
Resolution	16 bits
Number of channels	16 single-ended / 8 differential, switch selectable
Input ranges ▪ Gain is software selectable ▪ Unipolar/Bipolar polarity is switch selectable	±10V, ±5V, ±2.5V, ±1.25V 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D Pacing (software programmable)	Internal counter - 82C54. Positive or negative edge, jumper selectable.
	External source (pin25), positive or negative edge, software selectable.
	Software polled
A/D Trigger (only available when internal pacing selected, software enable/disable)	External edge trigger (pin 25), Positive or negative edge, software selectable.
A/D Gate (only available when internal pacing selected, software enable/disable)	External gate (pin 25), High or Low level, software selectable.
Simultaneous Sample and Hold Trigger	TTL output (pin 26), jumper enabled. Logic 0 = Hold, Logic 1 = Sample Compatible with CIO-SSH16
Burst Mode	Software selectable option, burst interval = 10uS
Data Transfer	From 1024 sample FIFO via interrupt w/ REPINSW
	Interrupt
	Software polled
Interrupt	INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9052
Interrupt polarity	Active high level or active low level, programmable through PLX9052
Interrupt Sources (software programmable)	End of Conversion
	FIFO not Empty
	End of Burst
	End of Acquisition
	FIFO Half Full
A/D conversion time	*10µs max*
Throughput	100KHz
Common Mode Range	±10V min
CMRR @ 60Hz	-100dB typ, -80dB min
Input leakage current	*±3nA max*
Input impedance	*10 MOhms min*
Absolute maximum input voltage	*+55/-40V fault protected via input mux*

Accuracy

Typical Accuracy	±2.3 LSB
Absolute Accuracy	±5.0 LSB
Accuracy Components	
Gain Error	Trimmable by potentiometer to 0
Offset Error	Trimmable by potentiometer to 0
PGA Linearity Error	*±1.3 LSB typ , ±10.0 LSB max*
Integral Linearity Error	±0.5 LSB typ , ±3.0 LSB max
Differential Linearity Error	*±0.5 LSB typ, ±2.0 LSB max*

Each PCIM-DAS1602/16 is tested at the factory to assure the board's overall error does not exceed ±5 LSB.

Total board error is a combination of gain, offset, differential linearity and integral linearity error. The theoretical absolute accuracy of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Analog input drift

Range	Analog Input Full-Scale Gain drift	Analog Input Zero drift	Overall Analog Input drift
±10.00V	2.2 LSB/°C max	1.8 LSB/°C max	4.0 LSB/°C max
±5.000V	2.2 LSB/°C max	1.9 LSB/°C max	4.1 LSB/°C max
±2.500V	2.2 LSB/°C max	2.0 LSB/°C max	4.2 LSB/°C max
±1.250V	2.2 LSB/°C max	2.3 LSB/°C max	4.5 LSB/°C max
0 - 10.00V	4.1 LSB/°C max	1.9 LSB/°C max	6.0 LSB/°C max
0 - 5.000V	4.1 LSB/°C max	2.1 LSB/°C max	6.2 LSB/°C max
0 - 2.500V	4.1 LSB/°C max	2.4 LSB/°C max	6.5 LSB/°C max
0 - 1.250V	4.1 LSB/°C max	3.0 LSB/°C max	7.1 LSB/°C max

Absolute error change per °C Temperature change is a combination of the gain and offset drift of many components. The theoretical worst case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Noise performance

The following table summarizes the worst case noise performance for the PCIM-DAS1602/16. Noise distribution is determined by gathering 50000 samples with inputs tied to ground at the PCIM-DAS1602/16 main connector. Data is for both Single-Ended and Differential modes of operation.

Range	±2 counts	±1 count	Max Counts	LSBrms*
±10.00V	97%	80%	11	1.7
±5.000V	97%	80%	11	1.7
±2.500V	96%	79%	11	1.7
±1.250V	96%	79%	11	1.7
0 - 10.00V	88%	65%	15	2.3
0 - 5.000V	88%	65%	15	2.3
0 - 2.500V	83%	61%	15	2.3
0 - 1.250V	83%	61%	16	2.4

* Input noise is assumed to be Gaussian. An RMS noise value from a Gaussian distribution is calculated by dividing the peak-to-peak bin spread by 6.6

Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the specified per channel rate for a total of 50000 samples. A full scale 100Hz triangle wave is input on channel 1. channel 0 is tied to analog ground at the 100 pin user connector. The table below summarizes the influence of channel 1 on channel 0 and does not include the effects of noise.

Range	1 kHz Crosstalk (LSB pk-pk)	10 kHz Crosstalk (LSB pk-pk)	50 kHz Crosstalk (LSB pk-pk)
±10.000 V	4	13	24
±5.000 V	2	7	18
±2.500 V	2	5	16
±1.250 V	3	4	14
0 V to +10.000 V	4	8	23
0 V to +5.000 V	2	5	16
0 V to +2.500 V	2	4	16
0 V to +1.250 V	3	3	16

Analog output

D/A converter type	MX7548
Resolution	12 bits
Number of channels	2
Channel type	Single-ended voltage output
Output range (jumper selectable per output)	±10 V, ±5 V, 0 to 10 V, or 0 to 5 V using on-board references, or user defined using external reference
Reference voltage (jumper selectable)	On-board, -10 V and –5 V
	External Independent (D/A0 pin 10 and D/A1 pin 26)
External reference voltage range	±10 V max
External reference input impedance	*10 KOhm min*
Data transfer	Programmed I/O
Throughput	System dependent. Using the Universal Library programmed output function (`cbAOut()`) in a loop, in Visual Basic, a typical update rate of 400 Khz can be expected on a 300 MHz Pentium II based PC.
Monotonicity	*Guaranteed monotonic over temperature*
Slew rate	2.0 V/µs min
Settling time	30 µS max to ±½ LSB for a 20 V step
Current drive	±5 mA min
Output short-circuit duration	*Indefinite @ 25 mA*
Output coupling	*DC*
Output impedance	0.1 ohms max
Output stability	Any passive load
Coding	Offset binary Bipolar mode: 0 code = Vref 4095 code = -Vref – 1LSB, Vref < 0V -Vref + 1LSB, Vref >0V Unipolar mode: 0 code = 0V, 4095 code = -Vref – 1LSB, Vref < 0V -Vref + 1LSB, Vref >0V
Output voltage on power up and reset	0 V ± 10 mV

Accuracy

Typical accuracy	±1 LSB
Absolute accuracy	±2 LSB
Accuracy Components	
Gain error	Trimmable by potentiometer to 0
Offset error	Trimmable by potentiometer to 0
Integral linearity error	±0.5 LSB typ, ±1 LSB max
Differential linearity error	*±0.5 LSB typ, ±1 LSB max*

Total board error is a combination of gain, offset, differential linearity and integral linearity error. The theoretical absolute accuracy of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Analog output drift

Analog output full-scale gain drift	±0.22 LSB/°C max
Analog output zero drift	±0.22 LSB/°C max
Overall analog output drift	±0.44 LSB/°C max

Absolute error change per °C temperature change is a combination of the gain and offset drift of many components. The theoretical worst case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Digital input / output

Digital I/O connector

Digital type	82C55
Number of I/O	24
Configuration per 82C55	2 banks of 8 and 2 banks of 4 or
	3 banks of 8 or
	2 banks of 8 with handshake
Input high	*2.0 volts min, 5.5 volts absolute max*
Input low	*0.8 volts max, -0.5 volts absolute min*
Output high	*3.0 volts min @ -2.5 mA*
Output low	*0.4 volts max @ 2.5 mA*
Power-up / reset state	Input mode (high impedance)
Pull-up/pull-down resistors	User installed. Dual footprint allows pull-up or pull-down configuration

Main connector

Digital output type	74LS244, power up / reset to LOW logic level
Digital input type	74LS373, pulled to logic high via 10 K resistors
Number of I/O	8
Configuration	4 fixed input, 4 fixed output
Output high	*2.7 volts @ -0.4 mA min*
Output low	*0.5 volts @ 8 mA max*
Input high	*2.0 volts min, 7 volts absolute max*
Input low	*0.8 volts max, -0.5 volts absolute min*

Counter

Counter type	82C54
Configuration	3 down counters, 16 bits each
Counter 1 source (software selectable)	▪ External source from main connector (pin 21*) ▪ 100 kHz internal source
Counter 1 gate	External gate from main connector (pin 24*)
Counter 1 output	Available at main connector (pin 2)
Counter 2 source (jumper selectable)	▪ Internal 1 MHz ▪ Internal 10 MHz
Counter 2 gate (software enable/disable)	External source from main connector (pin 25*)
Counter 2 output	Internal only, chained to counter 3 source
Counter 3 source	Counter 2 output
Counter 3 gate (software enable/disable)	External source from main connector (pin 25*)
Counter 3 output	Available at main connector (pin 20) Programmable as ADC Pacer clock.
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*30 ns min*
Low pulse width (clock input)	*50 ns min*
Gate width high	*50 ns min*
Gate width low	*50 ns min*
Input high	*2.0 volts min, 5.5 volts absolute max*
Input low	*0.8 volts max, -0.5 volts absolute min*
Output high	*3.0 volts min @ -2.5 mA*
Output low	*0.4 volts max @ 2.5 mA*
Crystal oscillator frequency	10 MHz
Frequency accuracy	50 ppm

* Pins 21, 24, and 25 are pulled to logic high via 10K resistors.

Environmental

Operating temperature range	0 to 70°C
Storage temperature range	-40 to 100°C
Humidity	0 to 95% non-condensing

Mechanical

Card dimensions	PCI custom type card: 107 mm (H) x 18.5 mm (W) x 216 mm (L)

Main connector and pin out

Connector type	37 pin male "D" connector
Connector Compatibility	Identical to CIO-DAS1602/16 Connector

8-channel differential mode pin out

Pin	Signal Name	Pin	Signal Name
1	+5V PC BUS POWER	20	CTR 3 OUT
2	CTR 1 OUT	21	CTR 1 CLOCK IN
3	DIG OUT 3	22	DIG OUT 2
4	DIG OUT 1	23	DIG OUT 0
5	DIG IN 3	24	DIG IN 2 / CTR1 GATE
6	DIG IN 1	25	DIG IN 0 / EXT TRIG / EXT PACER / EXT GATE
7	DIG GND	26	D/A1 REF IN / SS&H OUT
8	-5V REF OUT	27	D/A 1 OUT
9	D/A 0 OUT	28	AGND
10	D/A0 REF IN	29	AGND
11	CH7 LO	30	CH7 HIGH
12	CH6 LO	31	CH6 HIGH
13	CH5 LO	32	CH5 HIGH
14	CH4 LO	33	CH4 HIGH
15	CH3 LO	34	CH3 HIGH
16	CH2 LO	35	CH2 HIGH
17	CH1 LO	36	CH1 HIGH
18	CH0 LO	37	CH0 HIGH
19	AGND		

16-channel single-ended mode pin out

Pin	Signal Name	Pin	Signal Name
1	+5V PC BUS POWER	20	CTR 3 OUT
2	CTR 1 OUT	21	CTR 1 CLOCK IN
3	DIG OUT 3	22	DIG OUT 2
4	DIG OUT 1	23	DIG OUT 0
5	DIG IN 3	24	DIG IN 2 / CTR1 GATE
6	DIG IN 1	25	DIG IN 0 / EXT TRIG / EXT PACER / EXT GATE
7	DIG GND	26	D/A1 REF IN / SS&H OUT
8	-5V REF OUT	27	D/A 1 OUT
9	D/A 0 OUT	28	AGND
10	D/A0 REF IN	29	AGND
11	CH15 HIGH	30	CH7 HIGH
12	CH14 HIGH	31	CH6 HIGH
13	CH13 HIGH	32	CH5 HIGH
14	CH12 HIGH	33	CH4 HIGH
15	CH11 HIGH	34	CH3 HIGH
16	CH10 HIGH	35	CH2 HIGH
17	CH9 HIGH	36	CH1 HIGH
18	CH8 HIGH	37	CHO HIGH
19	AGND		

Digital input / output connector and pin out

Connector type	40 pin header
Connector Compatibility	Identical to CIO-DAS1602/16 Connector

Pin	Signal Name	Pin	Signal Name
1	NC	2	+5V PC BUS POWER
3	NC	4	DIG GND
5	PORT B 7	6	PORT C 7
7	PORT B 6	8	PORT C 6
9	PORT B 5	10	PORT C 5
11	PORT B 4	12	PORT C 4
13	PORT B 3	14	PORT C 3
15	PORT B 2	16	PORT C 2
17	PORT B 1	18	PORT C 1
19	PORT B 0	20	PORT C 0
21	DIG GND	22	PORT A 7
23	NC	24	PORT A 6
25	DIG GND	26	PORT A 5
27	NC	28	PORT A 4
29	DIG GND	30	PORT A 3
31	NC	32	PORT A 2
33	DIG GND	34	PORT A 1
35	+5V PC BUS POWER	36	PORT A 0
37	DIG GND	38	NC
39	NC	40	NC

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